Overview of the KORRIGAN project

Key Organisation for Research in Integrated Circuits in GaN Technology

Authors: Philippe Duême (SLIE), Thales Airborne Systems _ France,
Andrew Phillips, WP leader (System Impact), Phconsult for Selex-Galileo _ UK
Trevor Martin / David Wallis, SP leader (Material), QinetiQ _ UK
Antonio Cetronio, SP leader (Processing), Selex-SI _ Italy
Enrico Zanoni, SP leader (Reliability), University Padova _ Italy
Sylvain Delage, SP leader (Thermal Management), ATL3-5Lab _ France
Johan Carlert, SP leader (Demonstrators), Saab MS _ Sweden
Yves Mancuso, Thales Airborne Systems _ France
Iain Davies, Selex Galileo _ UK
Niklas Henelius, Norstel, _ Sweden
Marc Van Heijningen, TNO _ The Netherlands
Tibault Reveyrand, XLIM _ France

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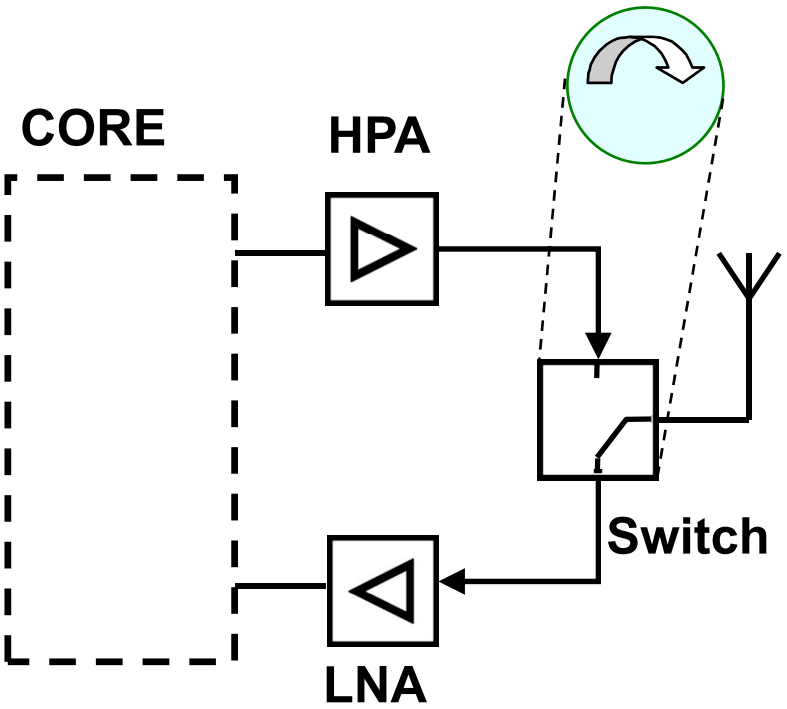
GaN in Europe before 2005

1. No simple route by which platform end users could gain exposure to GaN circuits
2. No clear supply chain from substrates - circuits
3. No opportunity to compare devices from different processes
4. No framework for understanding how to handle the high power densities associated with GaN
5. No unified approach to Reliability Assessment
6. No common approach to the development of GaN FET's for microwave systems

1. A route for platform end users



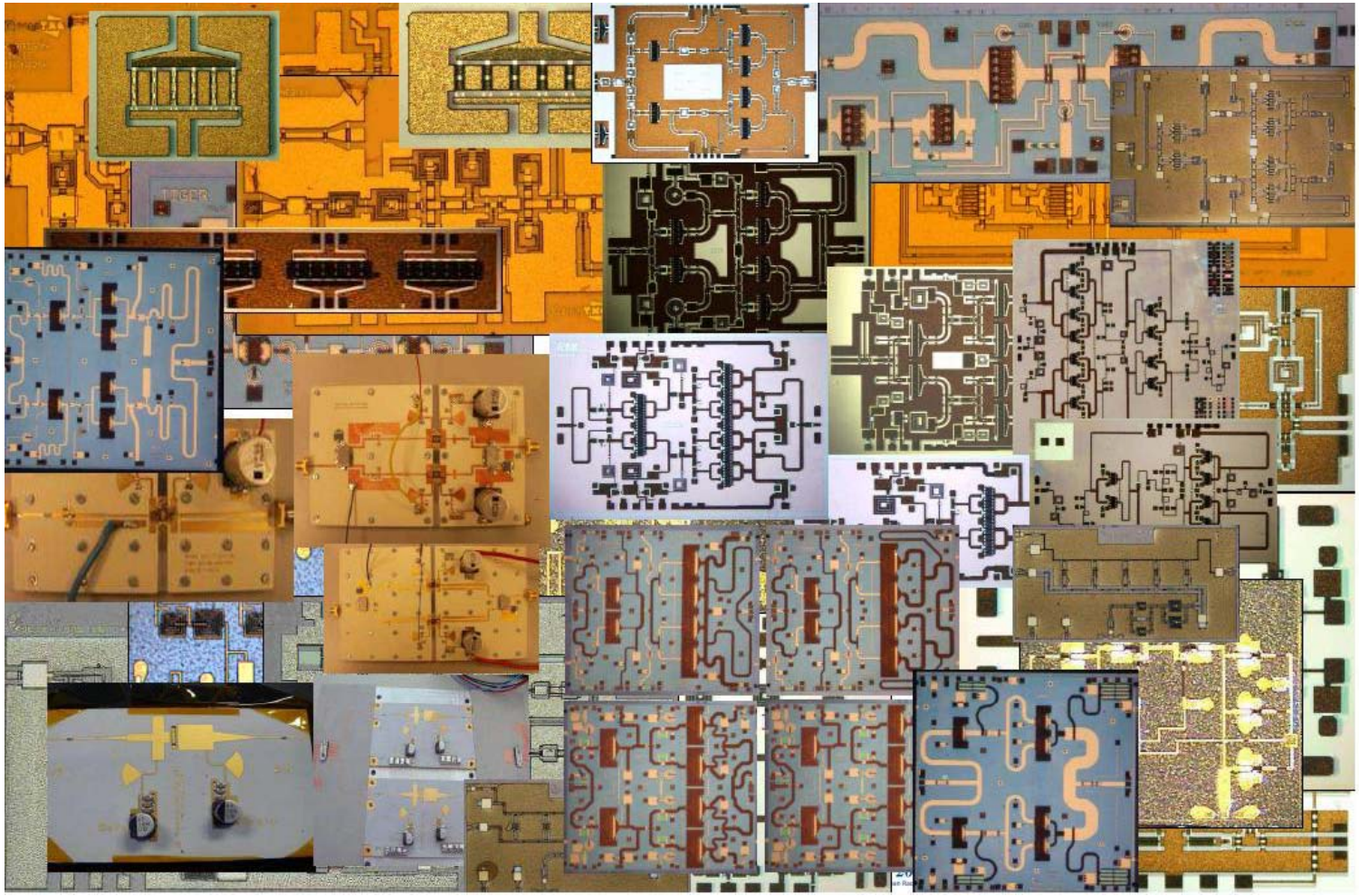
Demonstration on key applications X-band and Wideband Front End modules using GaN MMICs and advanced power assembly techniques

- High power density and robust HPA
- High power handling SPDT: Circulator replacement
- Robust LNA:
  No (less) limiting needed
- For EW:
  Wideband performance

MMIC Demonstrators

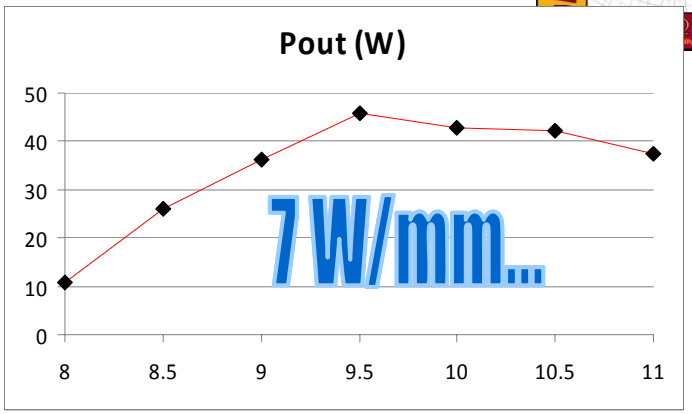
- Building blocks for radar and EW front-ends
- S-Band designs (3 GHz)
  - Power Bars for Hybrid HPAs
- X-Band Designs (8.5 - 10.5 GHz)
  - HPA MMICs
  - LNA MMICs
  - Switch MMICs
- Wide band designs
  - HPA MMICs (2-6 and 6-18 GHz)
  - LNA MMICs (2-18 GHz)
  - Switch MMICs (2-18 GHz)
- A total of 29 circuits demonstrators and 6 modules developed, more than in any programme world wide

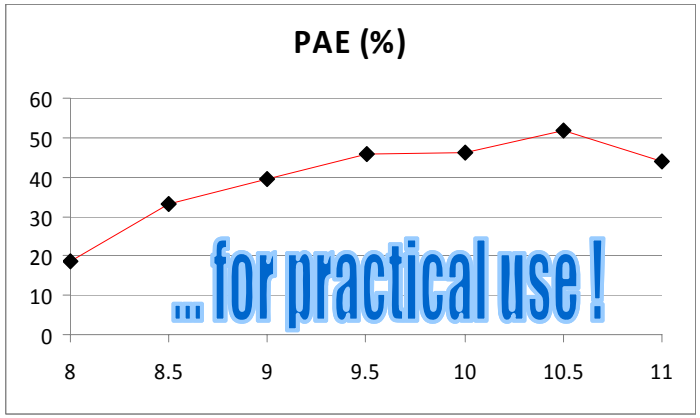
Unprecedented collection of GaN designs



2. A supply chain from substrates to circuits

- Korrigan addressed all the steps of the chain, many with more than one player:
  - Substrate (2”, 3”)
  - Epitaxy
  - Processing
  - Design guides and Model Library



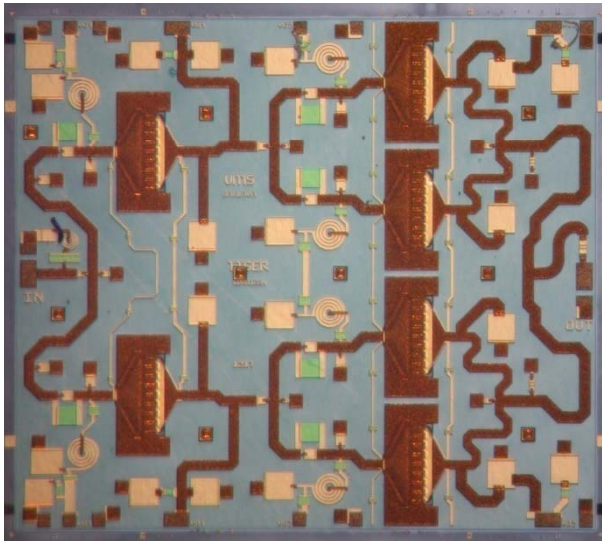


Freq (GHz)

2x16x100 µ (1st stage) 4x16x100 µ (2nd stage)

4300x3800 µm²

Pulsed drain 20µs / 200µs



Example of a 100% European achievement:
BAKLAVA X-Band amplifier (measurements)
NORSTEL wafer
QinetiQ Epitaxy
3-5 Lab process
UMS Design & OW Measurements

SiC semi-insulating substrates

- **Norstel AB established in 2005 to industrialise Okmetic/LiU SiC crystal growth**
- **Significant investements in SiC technology initiated in 2005, partly motivated by the Korrigan requirements**
  - **New custom-built facility commissioned in Norrköping, Sweden**
  - **New furnaces designed for 3" material and prepared for further diameter expansion**
  - **Complete wafering line**
  - **Extensive set of characterisation tools**

- **Regular deliveries of 2" SiC substrates from Norstel to the Korrigan team showing progressive improvement**
  - Polytype inclusions virtually eliminated
  - Micropipe density < 2 cm^{-2} demonstrated
  - Improved crystalline quality as shown by reduced contrast in crossed polariser images
  - Device level feedback so far indicates performance comparable to Cree substrates
- **3" substrates sampled**

- **Strategic collaboration Norstel / AIST (Japan) established (2007) for large-diameter high-quality SiC substrate development and manufacturing**
  - Long-term effort with first results expected in 2009

Epitaxy in Korrigan

- **Epitaxy activity in Korrigan had 3 main objectives**
  - **Supply of standard structures for processing**
  - **Diameter enlargement – from 2” to 3”**
  - **Development of advanced structures**

			Advanced structure development				
Epitaxy partner	**Growth of Korrigan std structures**	**Wafer diameters**	**AlN exclusion layers**	**Super lattice upper barriers**	**AlInN upper barriers**	**Double hetero-structure buffer layers**	**Fe-doping of buffer layers**
QinetiQ	✓	**2” & 3”**	✓			✓	✓
III-V Labs	✓	**2”**	✓		✓	✓	
Picogiga (MBE)	✓	**2” & 3”**	✓	✓		✓	
Linkoping University	✓	**2”, 3” & 4”**	✓			✓	
Lecce university	✓	**2”**	✓				

- **More than 250 epi-layers on SiC supplied for processing**
- **Yield of Korrigan std structures ≈90% for most partners in final stages of program**
  - Including growth on 3” substrates
- **Device benefits demonstrated for advanced structures in many cases**

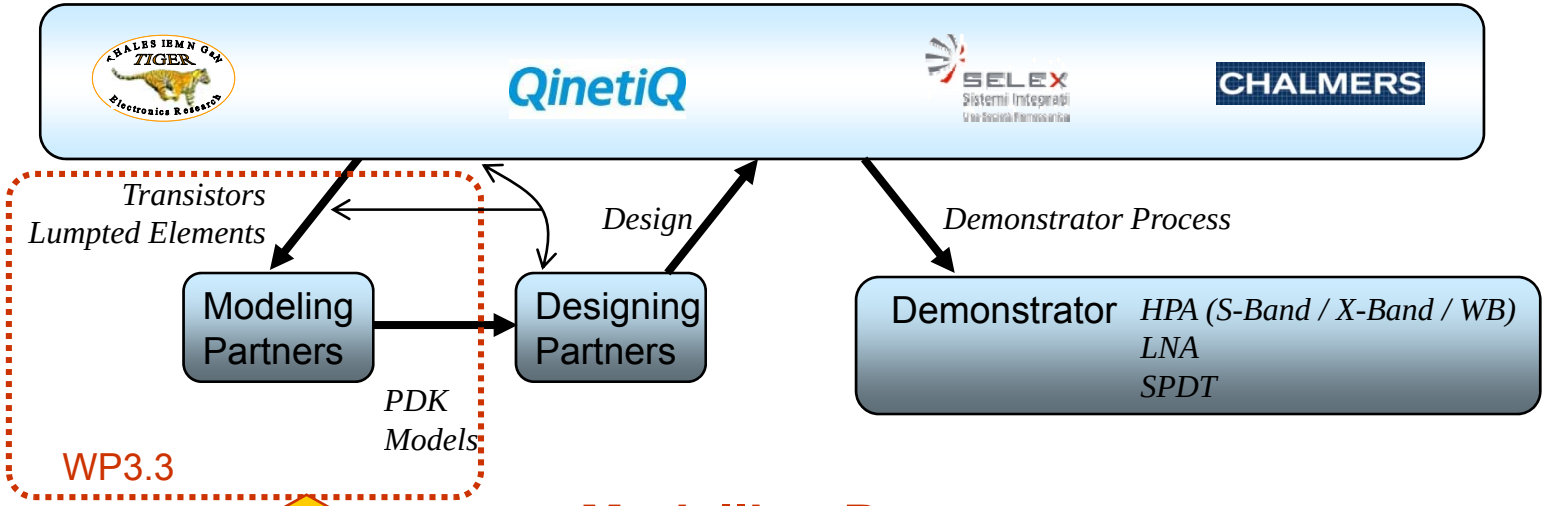
Korrigan standard wafer specification

Parameter	Value	Wafer to Wafer Variation
Surface particles and contamination	Zero particles> 10 microns high	
Upper barrier thickness (including GaN cap for MBE grown layers)	25nm	±10%
Channel carrier density	$1x10^{13}$ cm^{-2}	±10%
Channel sheet resistivity	420 ohms/sq	±10%
Vpinch	-5.2V	±20%
Isolation of GaN buffer layer	Insulating, No free carriers	<2pF 1Volt above pinch-off measured by HgCV @ <10kHz

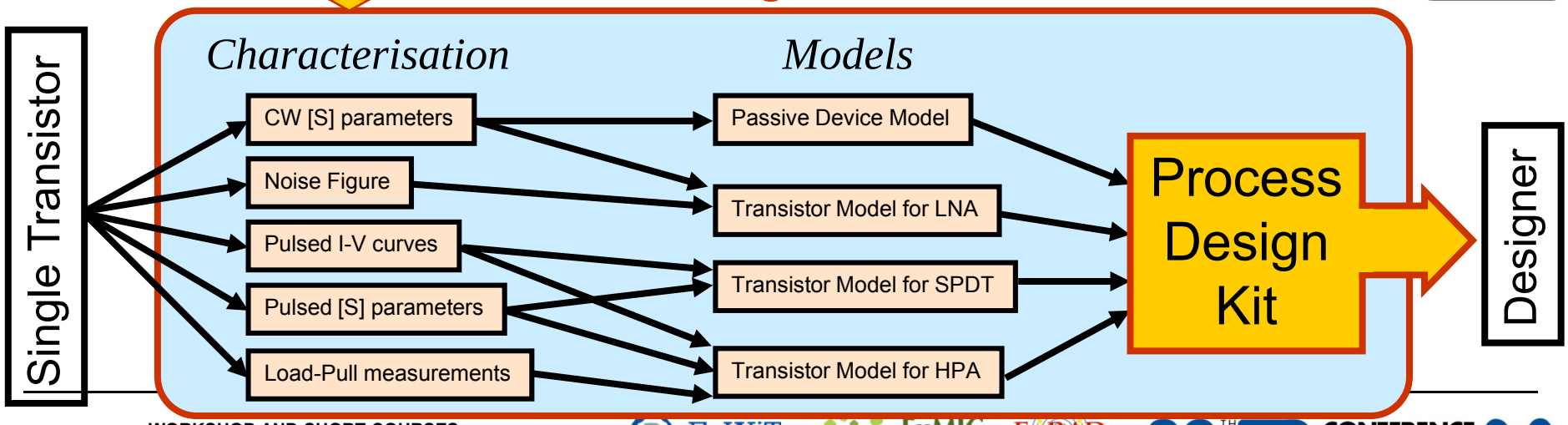
- Stable layer structure crucial to allow development of stable device processes
- Korrigan standard wafer specification defined at To+18
  - Allowed best practice in each lab to be used whilst giving a common electrical performance
  - Used for all MMIC circuits in Korrigan
- Significant activity undertaken to ensure measurement consistency across epitaxy partners
  - Common samples exchanged between 6 centres to validate material measurements (Hg CV, Al%, Rsheet..)
  - Best practice defined across laboratories

Modelling: Partnership

Four foundries are implied in Korrigan final demonstrators



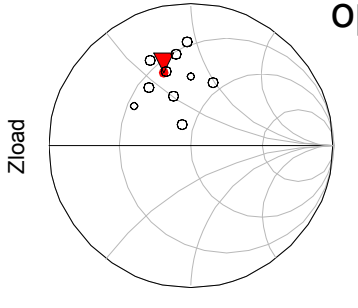
Modelling Process



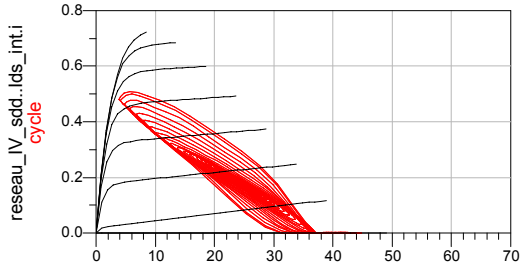
Modelling: Result example

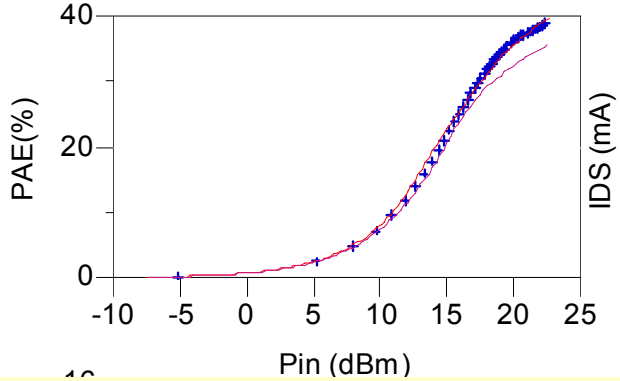
Modeling Trapping Effects at Large Signal

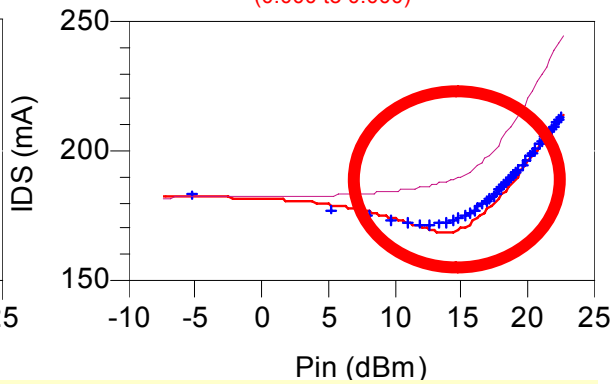
Traps ON
Traps OFF
Measurements

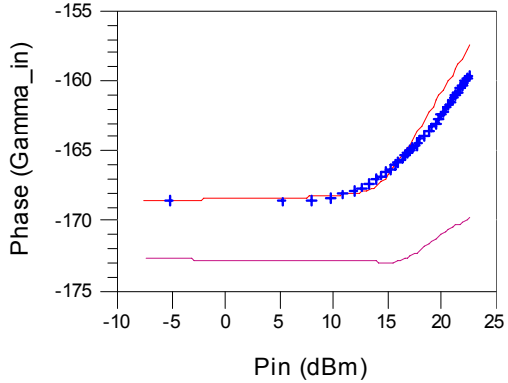


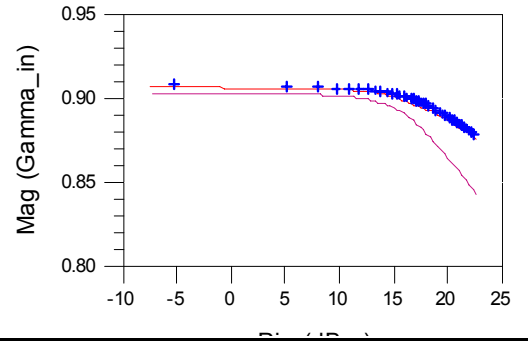
Measurements @ power optimal load impedance





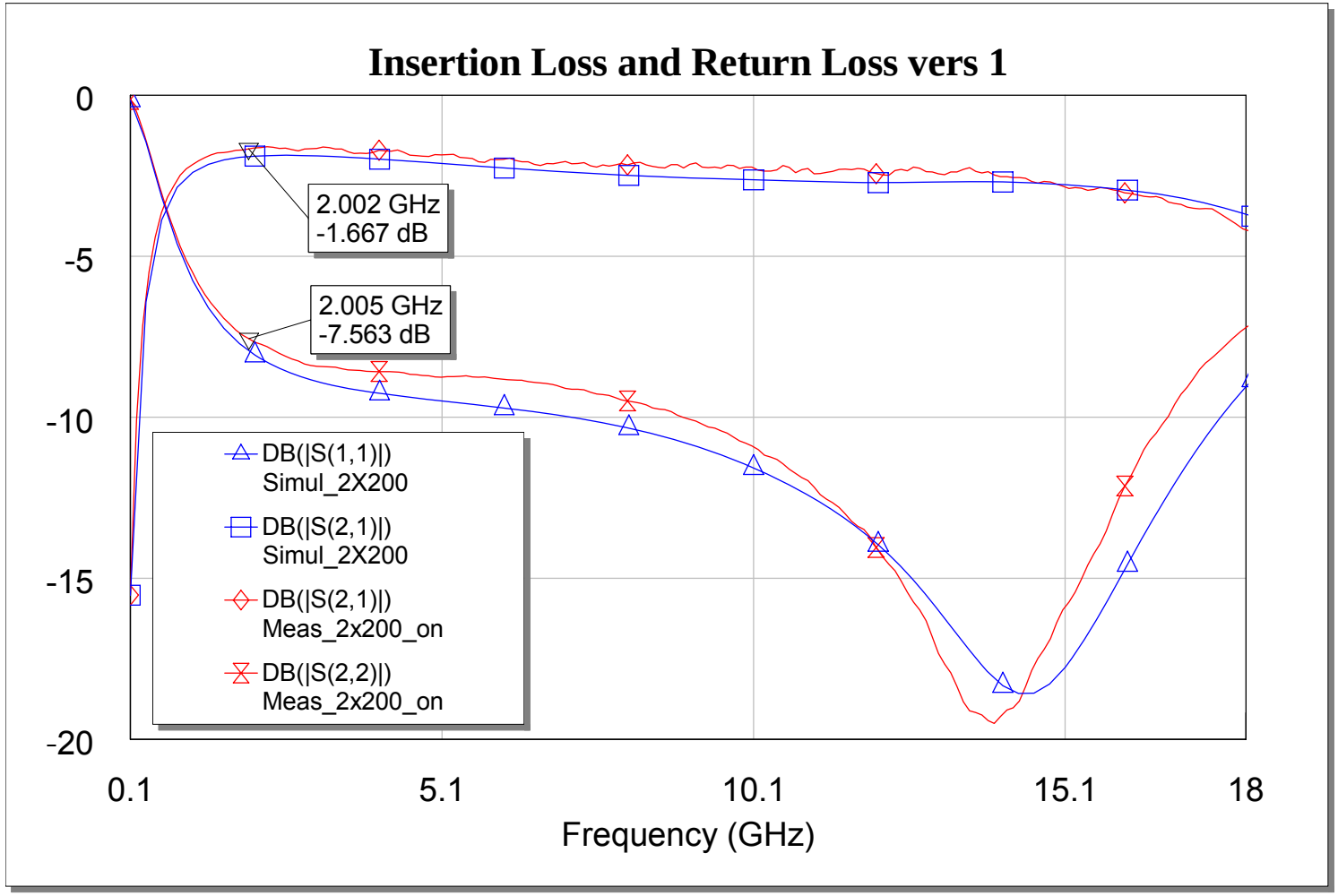




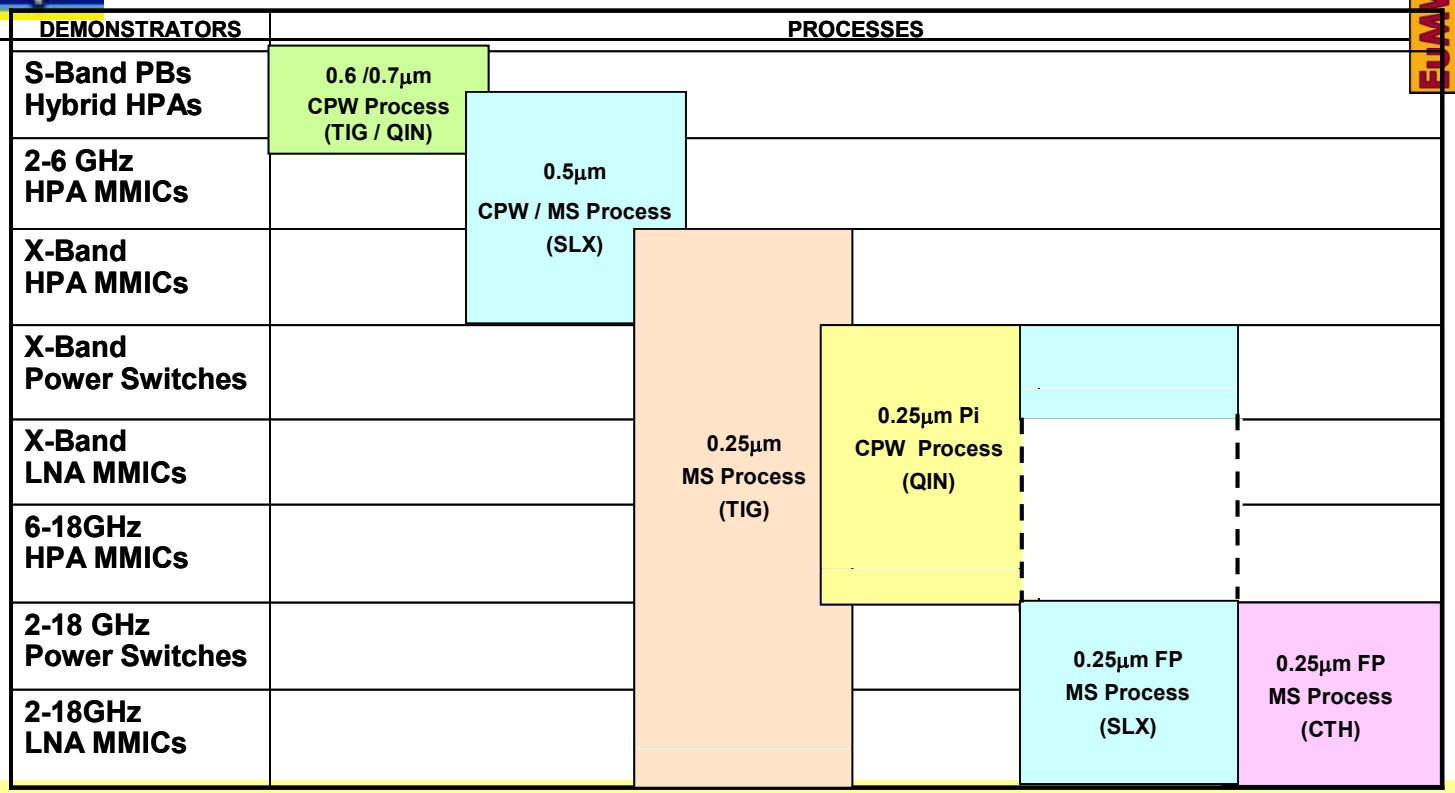


O. Jardel, F. De Groote, T. Reveyrand, J.C. Jaquet, C. Charbonniaud, J.P. Teyssier, D. Floriot, R. Quéré
«An electrothermal model for AlGaN/GaN Power HEMTs including trapping effects to improve large-signal simulation results on high VSWR»
IEEE Transactions on Microwave Theory and Techniques, Vol. 55, No 12, pp.2660-2669, December 2007.

Model accuracy illustrated by a WB Switch



3. An opportunity to compare devices from different processes

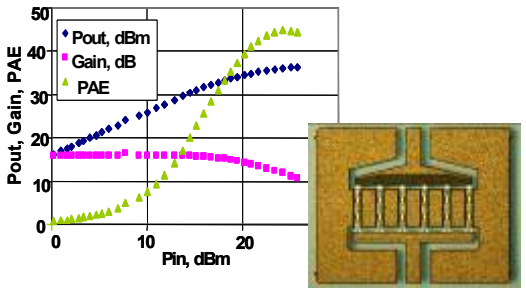


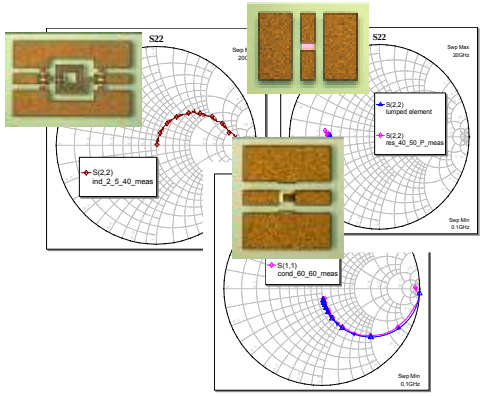
Six processes have been developed by KORRIGAN Foundries for Demonstrator fabrication

- 0.6/0.7µm Power for CPW Power Bars (QIN/TIG)
- 0.5µm Power CPW/MS (SLX)
- 0.25µm General Purpose MS (TIG)
- 0.25µm (T-gate) General Purpose CPW (QIN)
- 0.25µm (Field Plate) LNA/Switch MS (CTH)
- 0.25µm (Field Plate) LNA/Switch MS (SLX)

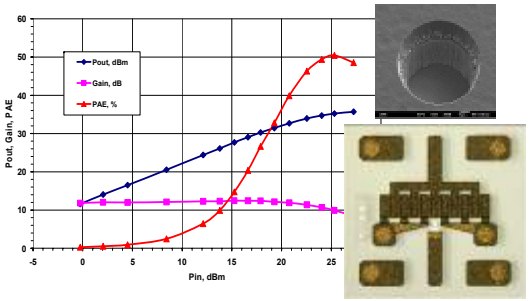
KORRIGAN Foundry DKs

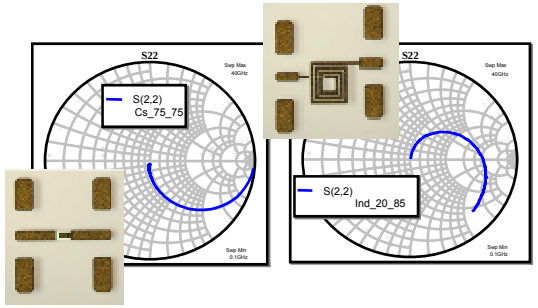
Co-Planar Waveguide Technology





Micro-Strip Technology





Active device library from 0.1 to 2.4mm gate-width for small-signal, switching and power applications

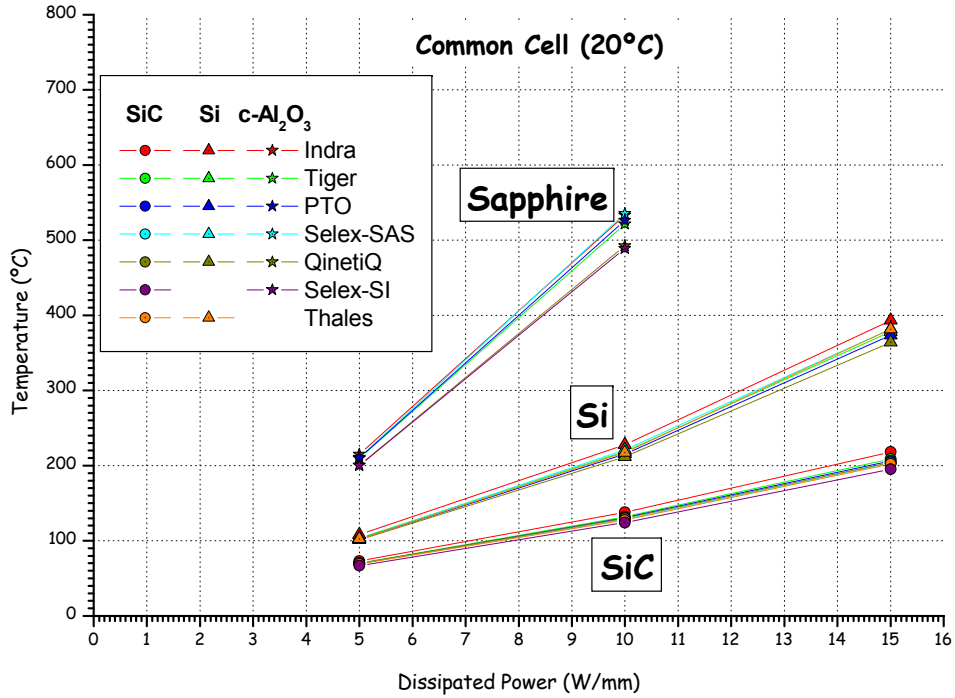
Passive component library composed of high voltage breakdown MIM capacitors, inductors and thin-film resistors

Foundry PDKs on KORRIGAN web-site for ADS and AWR workstations

4. A framework for understanding and managing thermal issues with GaN

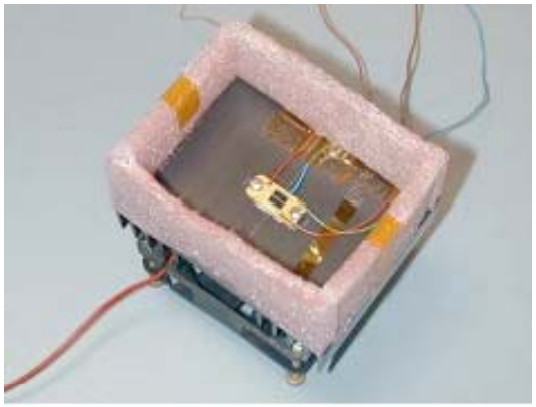
- Definition of a common cell for tool validation
- Simulation parameters / simplifications
- Stationary and transient simulations
- Comparison of simulations with real measurements

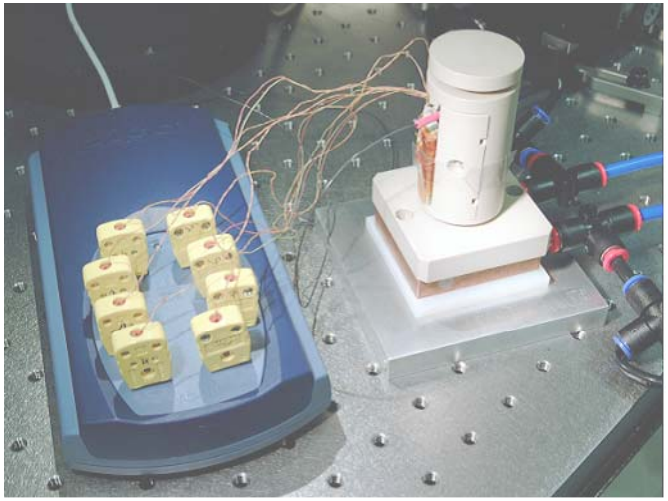
Very good agreement for all partner's results and experimental measurements



Advanced Assembly Technologies

Thermal and physical test performed on various assembly stack-up

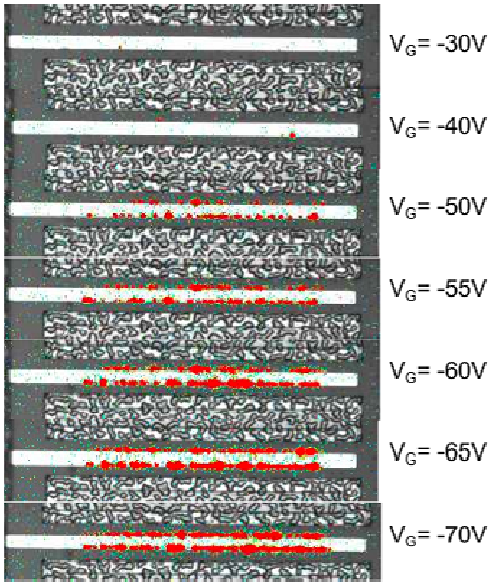


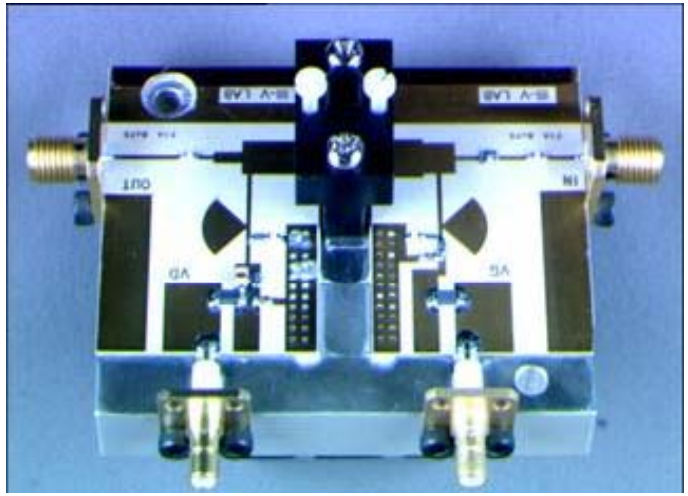


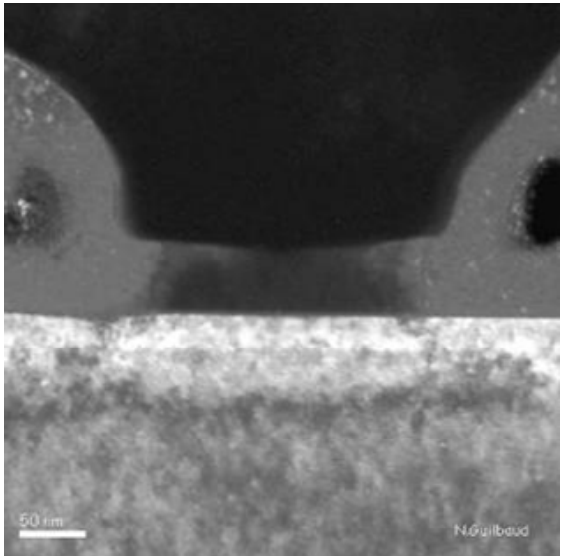
* These measurements have been performed on test chips designed and manufactured at the beginning of the project with the only scope of optimization of the flip chip process, the electrical characteristics of these devices are not at the state of the art of GaN technology.

5. A unified approach to reliability assessment

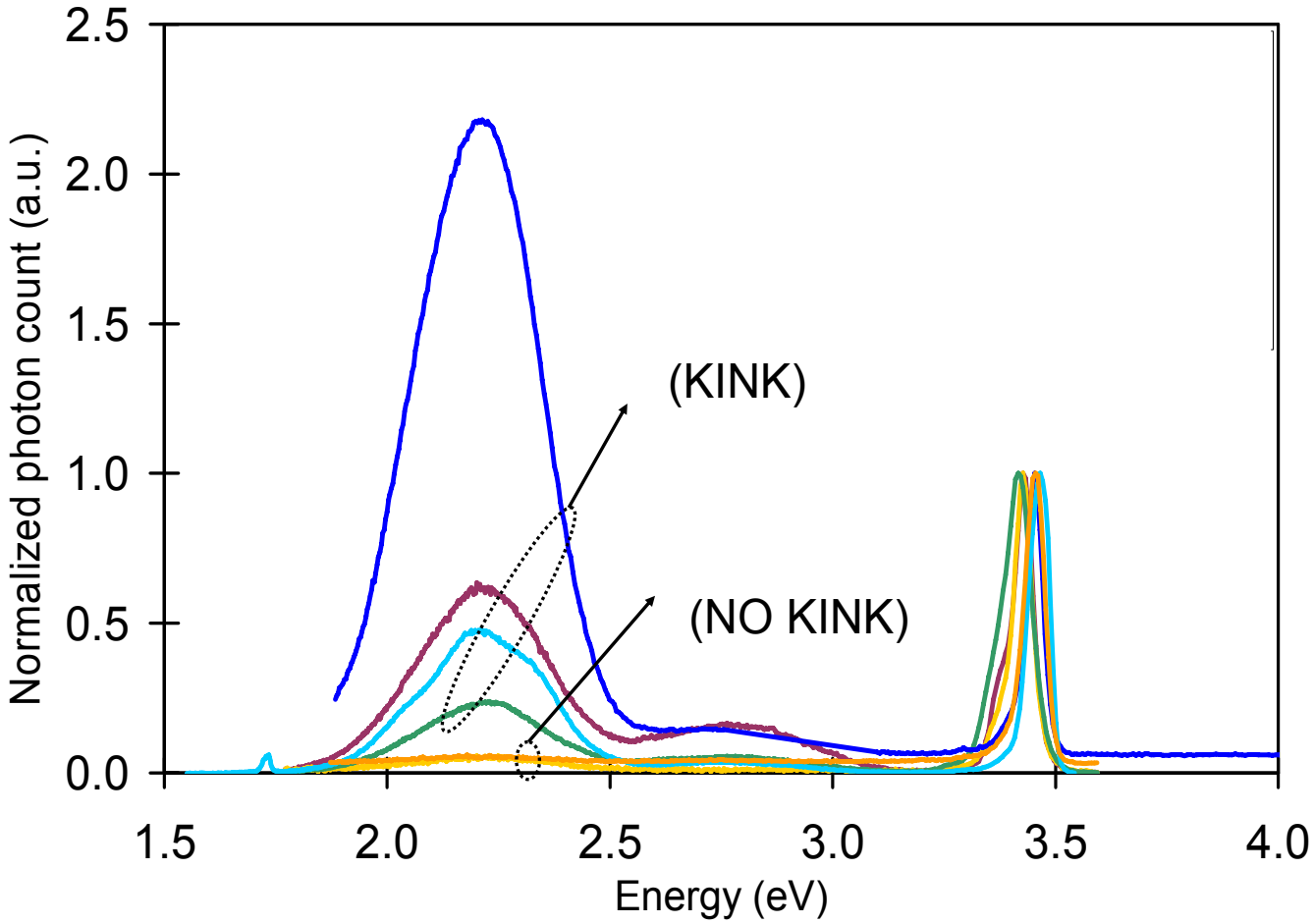
- A unique database containing data related to more than 30 wafes, 400000 device-hours
- Approximately 20 long-term accelerated life tests exceeding 1000 hours and a large number of short-term reliability experiments
- A methodology for the study of trap-induced effects
- Main failure modes and mechanisms of AlGaN/GaN HEMT's identified
- First analysis of correlation between DC aging and rf aging





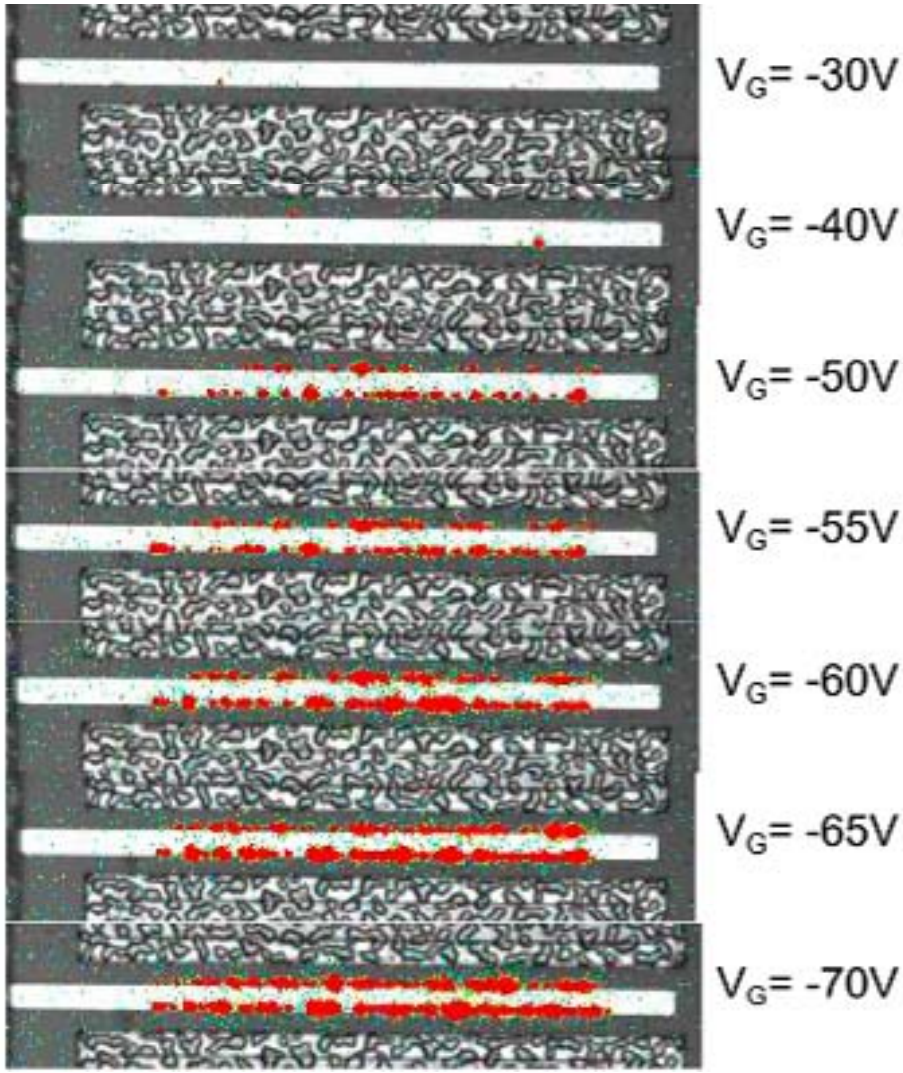


Screening of wafer affected by kink using cathodoluminescence



Damage creation in the AlGaN due to high Vgd

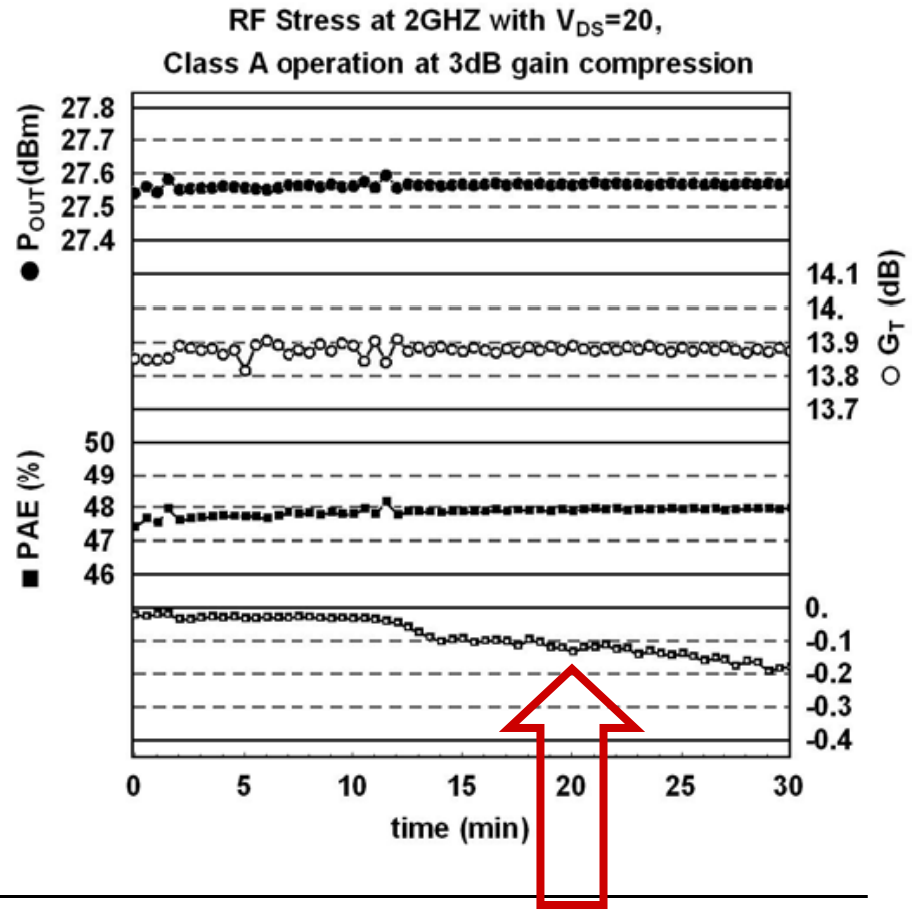
Step stress experiment from VGSD = -15 V to -100 V (or failure) 2 minutes long



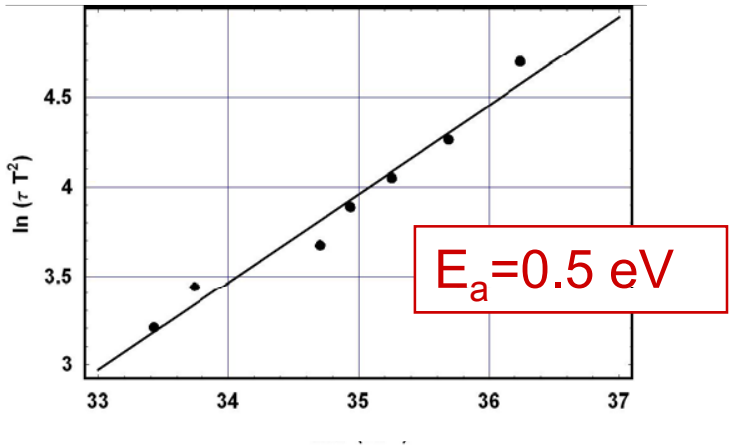
Electroluminescence measured at VGDS=-10 V after each step

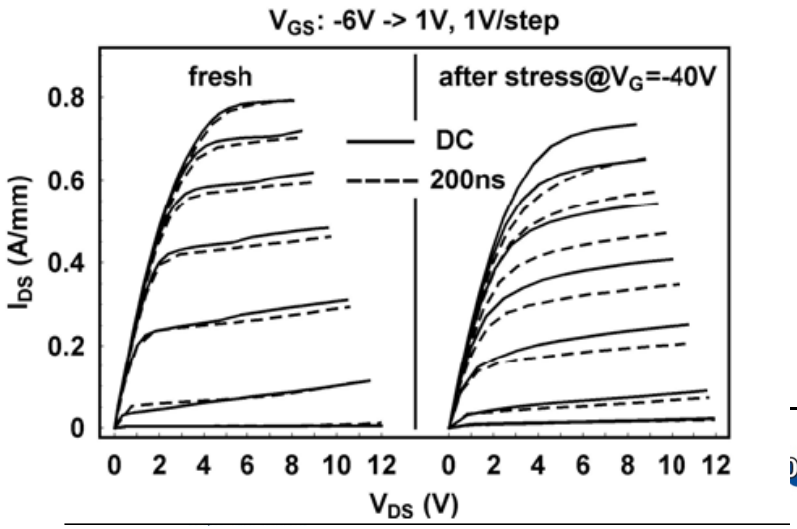
Correlation DC – rf stress

RF stress (quiescent point class A operation, 50% of IDSS, biased at 10V, matched for maximum output power and then driven 3dB into compression for 30 minutes. RF stress carried out by increasing the drain bias by 5V every 30 minutes.



gate current increase



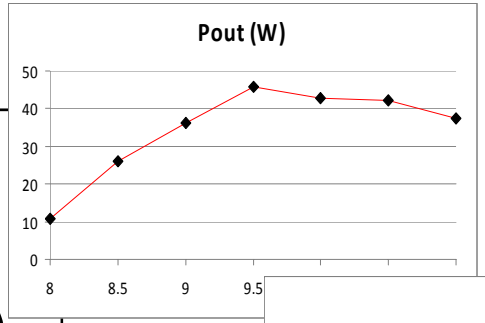


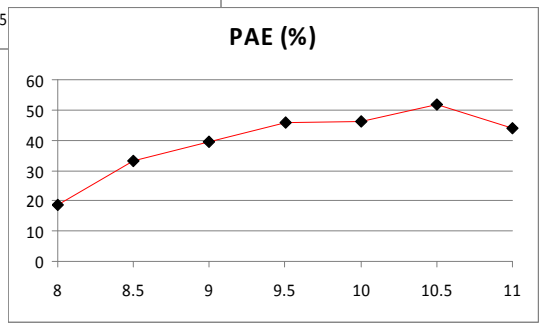
6. A common approach to the development of GaN FET's for microwave systems

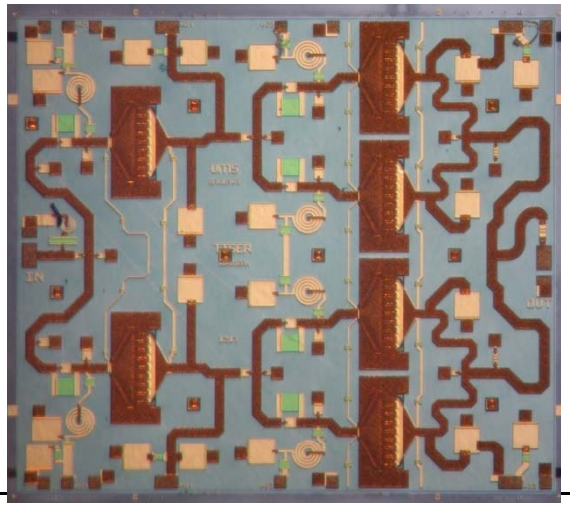
- A robust supply chain has been established, from substrates through foundries to circuits.
- The establishment of common procedures such as a common PCM, design rules, FDR procedure and reliability testing allows different processes and devices to be directly compared
- Complete Model Library, on a generally accessible WEB site
- A large database for reliability and parasitic effects is available
- Unified approach to thermal modelling and simulation

Some selection of Korrigan Demonstrators

- **S-Band designs (3 GHz)**
  - Power Bars for Hybrid HPAs
- **X-Band Designs (8.5 - 10.5 GHz)**
  - HPA MMICs
  - LNA MMICs
  - Switch MMICs
- **Wide band designs**
  - HPA MMICs (2-6 and 6-18 GHz)
  - LNA MMICs (2-18 GHz)
  - Switch MMICs (2-18 GHz)
    Wideband and X-Band modules



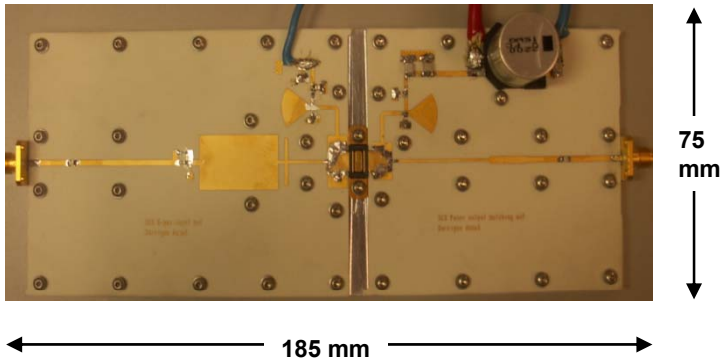




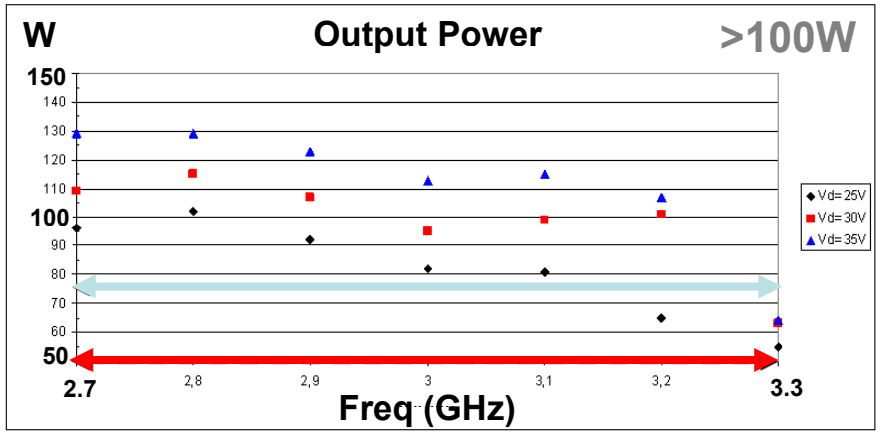
S-Band Hybrid HPA - SMW

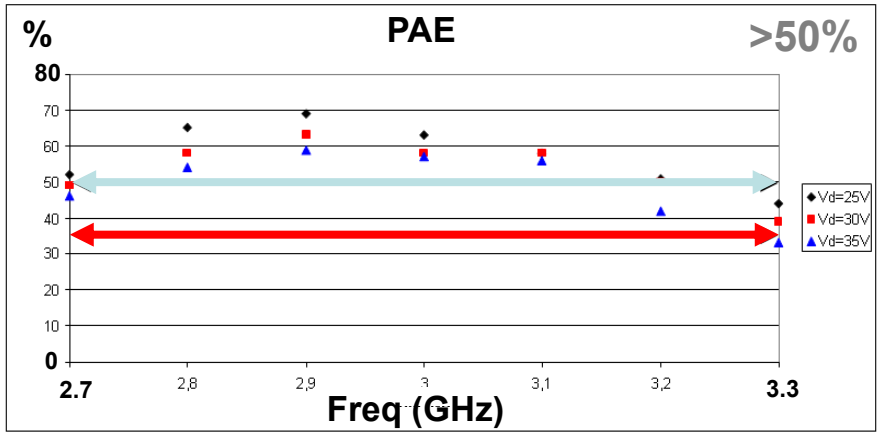
Foundry: SELEX-SI / Design: SAAB

- **Technology process:** AlGaN/GaN/SiC Lg = 0.5µm (CPW)
- **Design approach:** Single stage HPA
  - Gate periphery: 2 x 9.6 mm power bars mounted in parallel into one package.
  - Substrate: Rogers 4350 (εr = 3.66)



Pout & **PAE** vs Frequency @ 25, 30 & 35 V, duty cycle = 5%, pulse width = 50µs

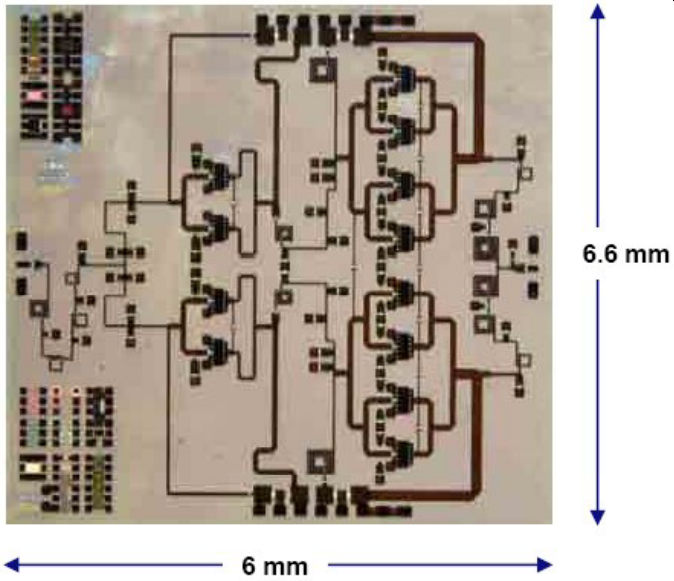


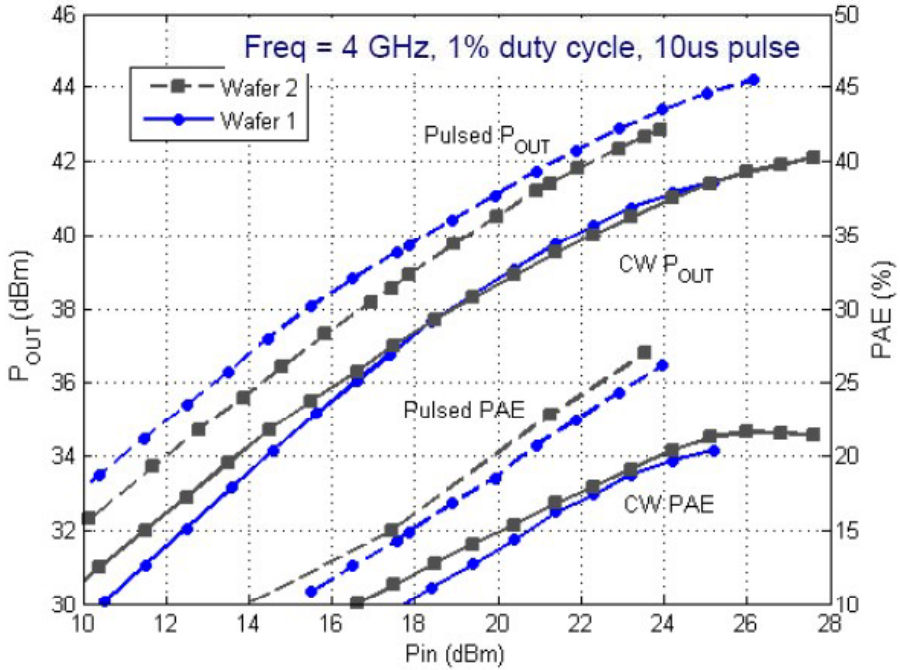


2-6 GHz Wideband HPA

(SLX technology, INDRA design)

- **Technology process:** AlGaN/GaN/SiC Lg = 0.5 µm
- **Design approach:** Two-stage HPA
  - gate periphery: 4x1 mm first stage, 8x1 mm output stage
  - 1 mm (10 x 100 µm) unit cell

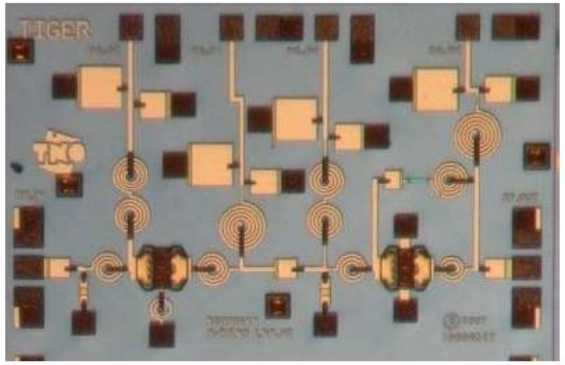




- **Measurements:**
  - Vds = 25 V,
  - CW and pulsed measurements on test-jig
  - Pulsed Pout = 44 dBm with >26% PAE
  - Linaear Gain = 12 .. 20 dB, 2-6 GHz

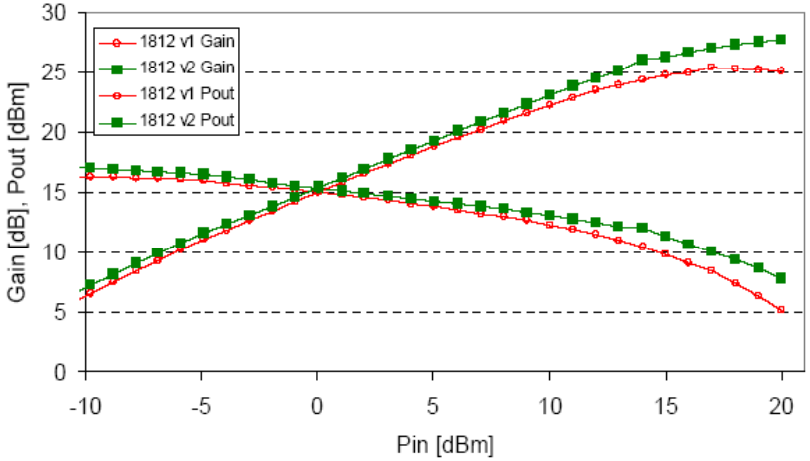
X-band LNA

(Tiger III-V lab technology, TNO design)

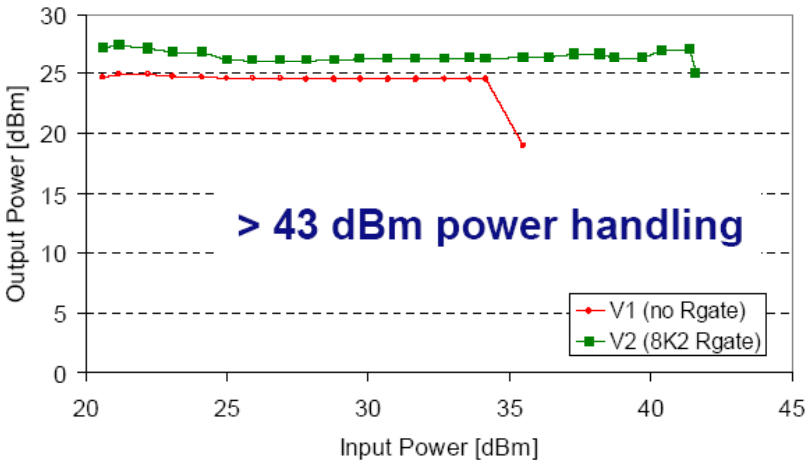


- **Technology process:** AlGaN/GaN/SiC Lg = 0.25 µm
- **Design approach:** Two-stages, 4x50um / 4x75um FETs
- Noise Figure = 2.5 dB (Simulated 1.5 dB)
- Gain = 17 dB (corresponds with simulation)

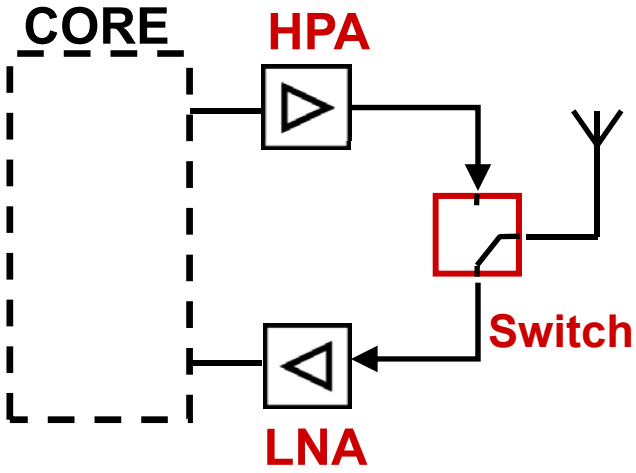
CW power sweep, compression measurement



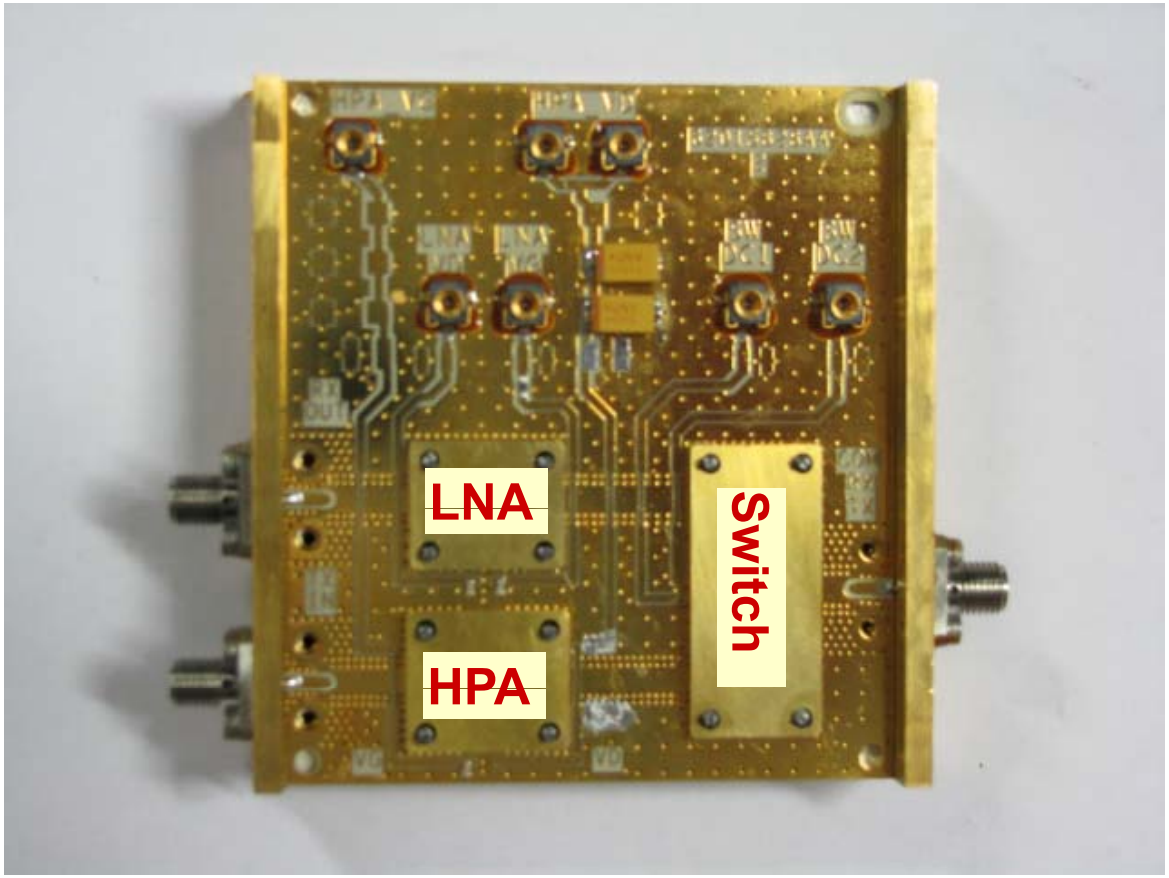
5 µs pulse-width, 10 % duty cycle, Input power survivability measurement



Module Demonstrators: X-Band Front End



Integration of 3 Korrigan MMICs

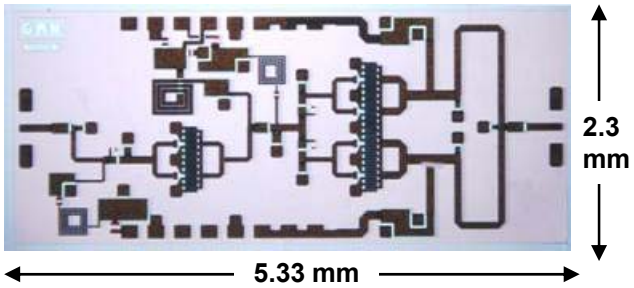


- **Foundry**:
  - ATL III-V Lab
- **Circuit Design:**
  - TNO, UMS
- **Module Design:**
  - Thales Airborne Systems

Module Demonstrators: X-Band packaged HPA

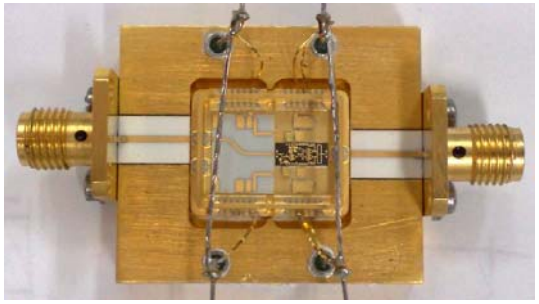
Microstrip MMIC HPA

Design: SELEX-SI / Foundry: SELEX-SI



Packaged HPA

Design: SELEX-SI



Test conditions: Drain Bias Voltage=20V, Pulse Width=100µs; Duty Cycle=25%, Baseplate Temperature=25˚C.

HPA mounted on test jig:

Frequency = 9 GHz

- Linear Gain = 17 dB

@3dB compression point:

- Output Power = 15 W
- PAE = 40%

Packaged HPA in test fixture:

Frequency = 9 GHz

- Linear Gain = 16 dB

@3dB compression point:

- Output Power = 13.5 W
- PAE = 36%

Module Demonstrators: Air cooled S-Band HPA

Air cooled strategy for GaN

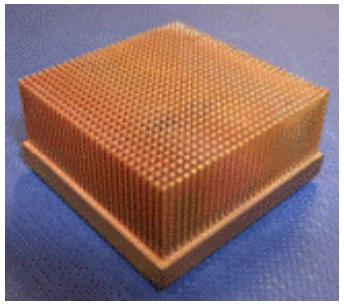
•Air cooling of amplifier modules is achieved by incorporating air cooling channels, with high surface area to volume ratio heatsinks, into module package structures.

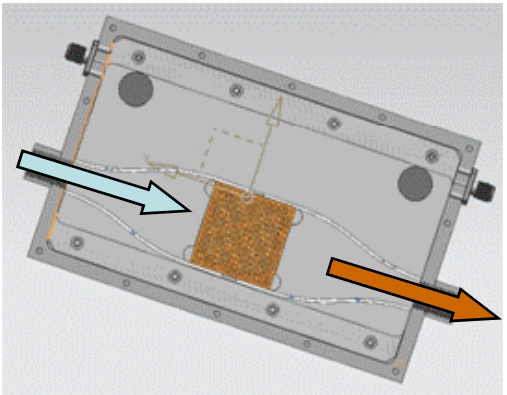
•Effective cooling can be achieved with low air flowrates which minimises the prime power requirement of fans. This is important for systems with large numbers of amplifiers.

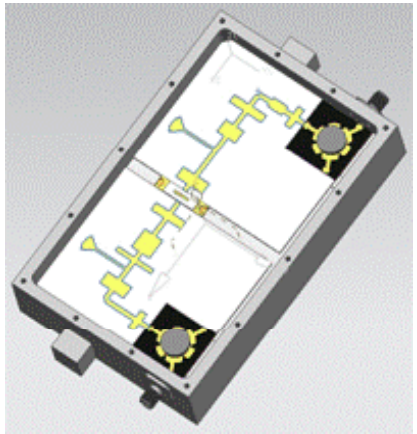
•Low cooling air flowrates result in low system operating pressures.

Typical example of a high surface area to volume ratio heatsink using pin fins.

Channel Width:	30mm
Channel Length:	30mm
Channel Height:	10mm
Pin Fin Cross Section:	0.5mm x 0.5mm
Pin Fin Pitch:	1mm

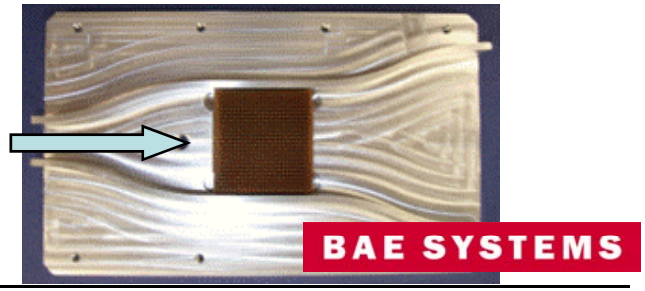






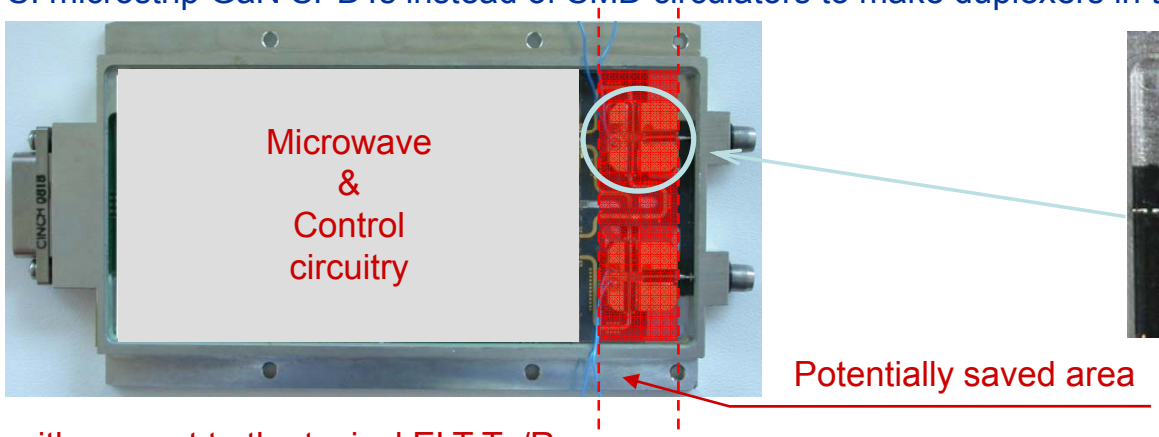
HPA module incorporating an enclosed air cooling channel with a compact forced cooled pin fin heatsink.

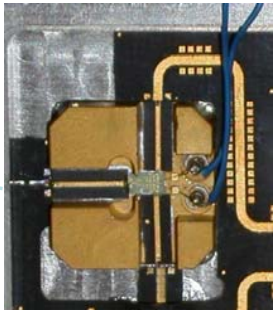
Photograph of thermal test rig showing cooling channel and amplifier heatsink.



Wide band Tx/Rx FE demonstrator

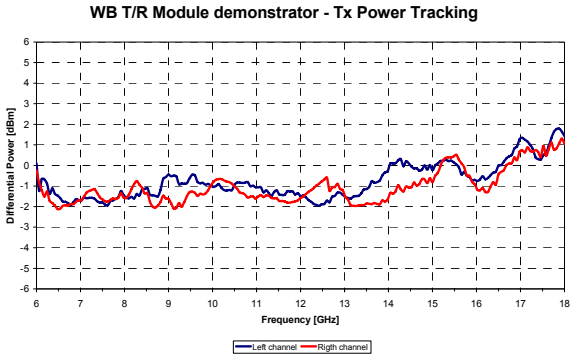
ELT/SELEX-SI microstrip GaN SPDTs instead of SMD circulators to make duplexers in the typical ELT 4W Tx/Rx

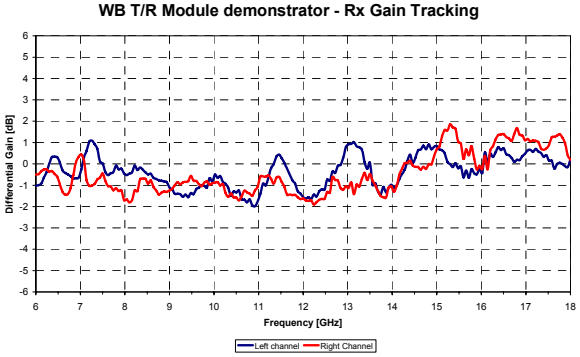


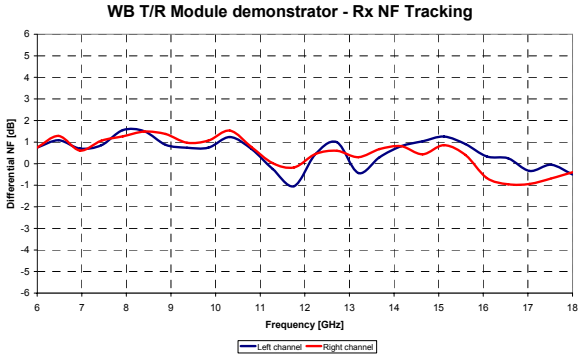


Achievements with respect to the typical ELT Tx/Rx :

- positive slope versus frequency performances
- Tx Pout, Rx gain and NF in average 1dB better @18GHz
- 15% size reduction potentially allowed, giving up to massive circulators







GaN SPDTs developed in KorriGaN already provide suitable alternatives to SMD circulators in the FE design, due to flat IL, rugged power handling, high isolation and very small size

Conclusion 1

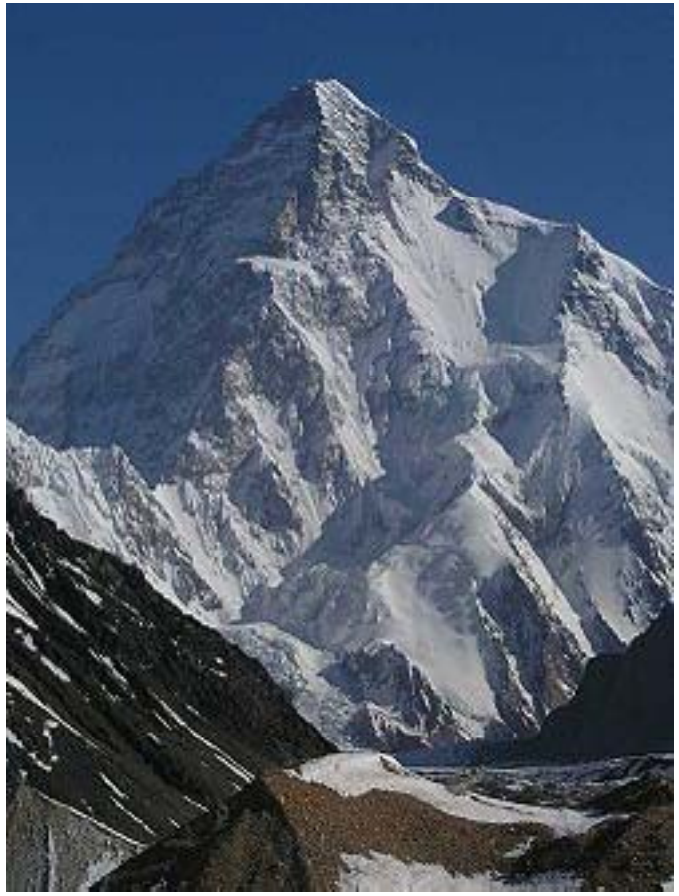
Korrigan achievement

- **Korrigan has taken the technology to a stage where circuit system designers can have a clear view of the potential of GaN, detailed guidance on the way the technology is used, and the detailed performance data needed to carry out simulations at the system level.**
- **Component availability: expected around 2011-2012**
- **Development and qualification for an expected operational use, in systems, around 2015-2020**

Conclusion 2

Prospective for continuation of the effort in Europe

A project on substrates / materials already on the tracks



- **Ongoing discussion on device-centred follow-up**